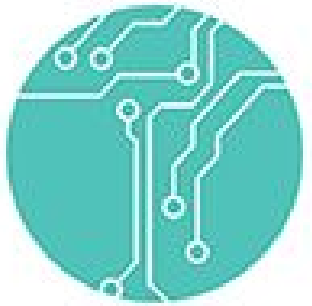


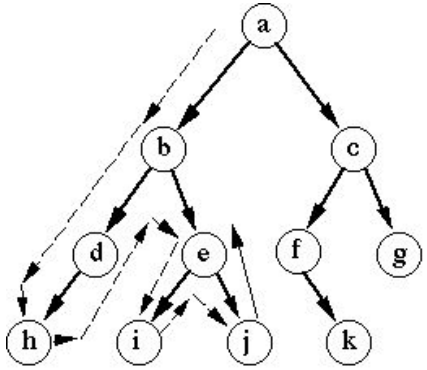


GraphAcc: FPGA-based computational accelerator for large-scale graphs

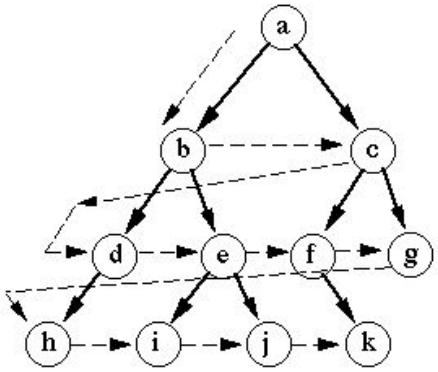
Liang Xu, xul4@vuc.edu
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Department of Electrical and Computer Engineering
Virginia Commonwealth University
Adviser: Dr. Weijun Xiao

Graph computing

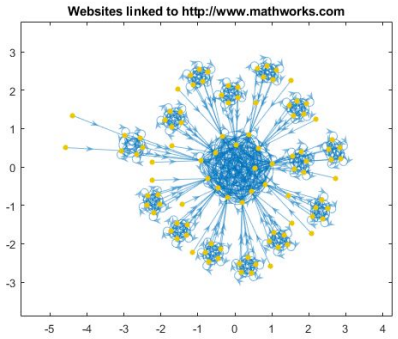
Many **real-world** scenarios and problems can be modeled as graphs.
Vertices: Objects and properties.
Edges: Relationships between objects.



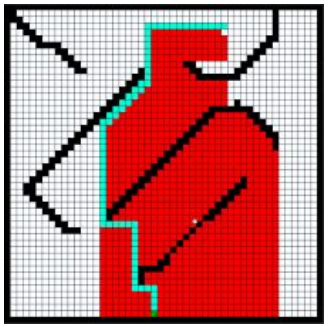
Depth First Search



Breadth First Search



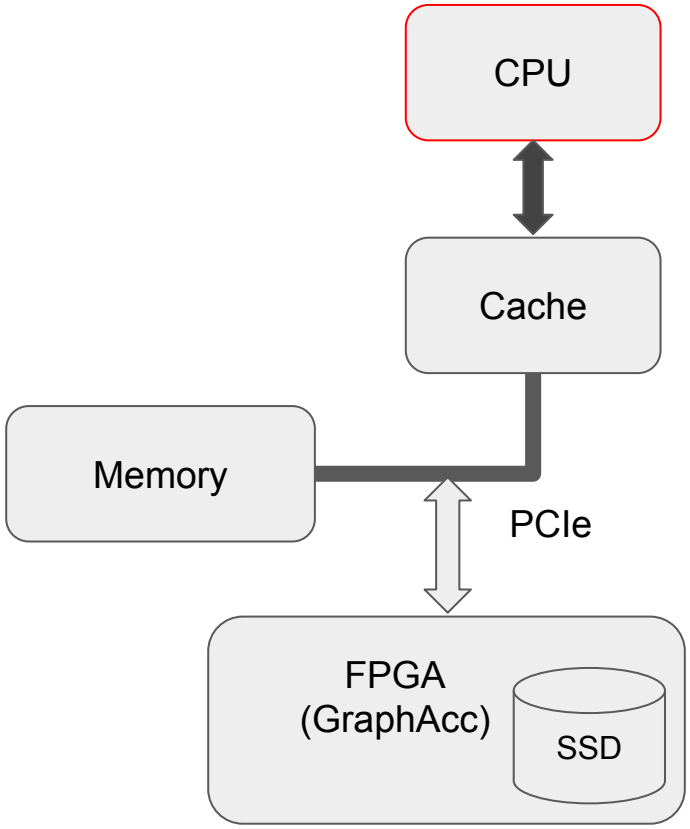
Page Ranking



A* Algorithm

Challenge	**Response**
Too large for memory	Use large storage (SSD).
High cache miss rate	Offload I/O.
Repeated preprocessing	Offload preprocessing.

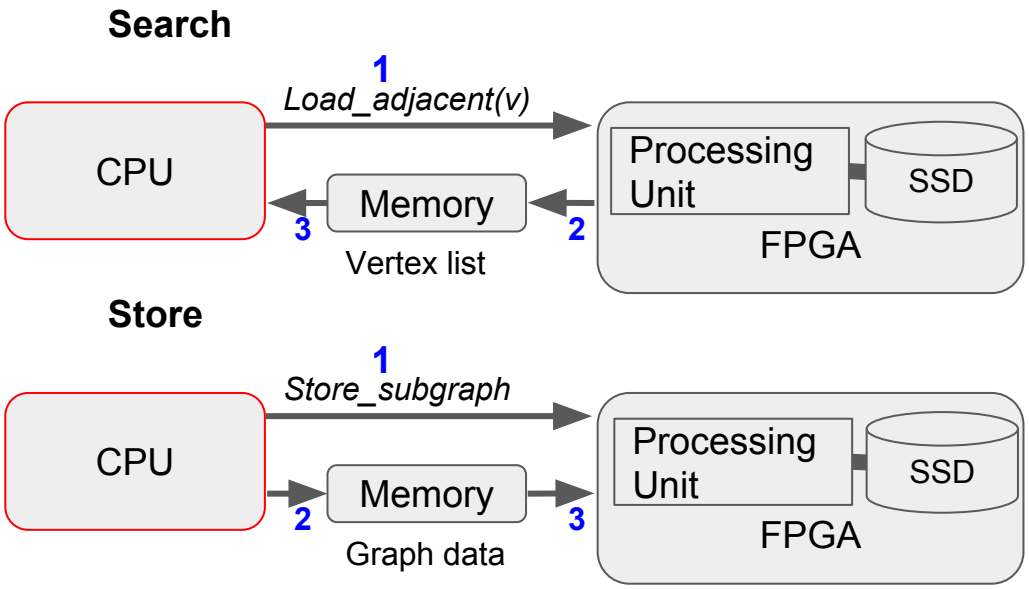
Proposed method



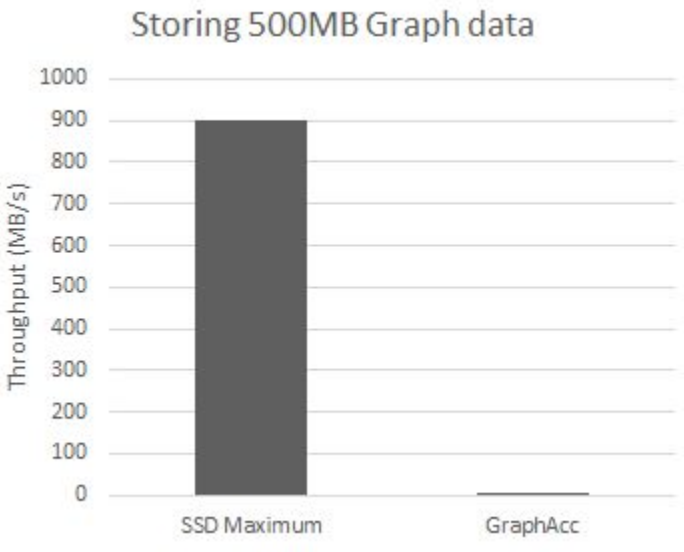
Host issues commands over PCIe.

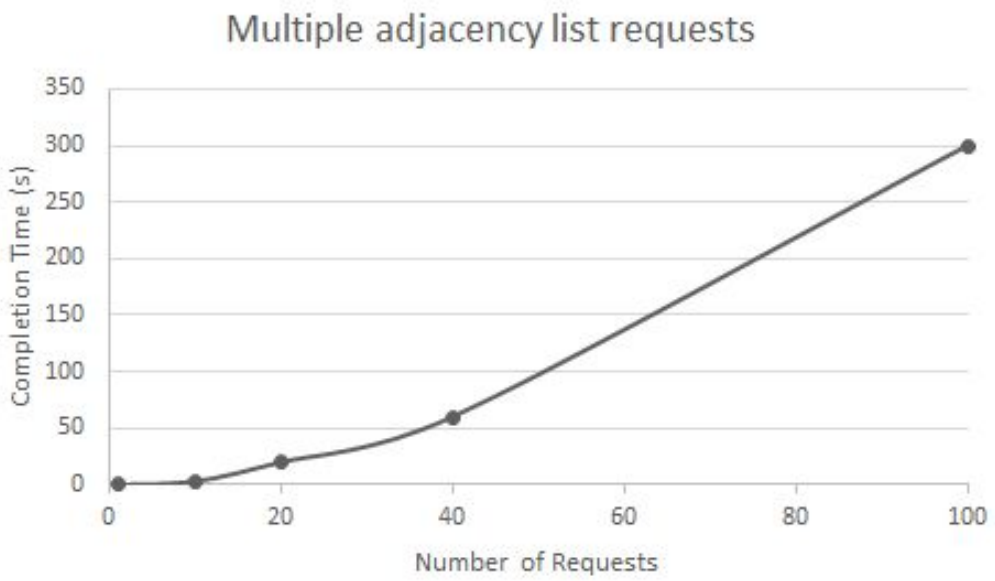
FPGA transfers graph data to or from main memory via DMA.

We can implement complex I/O schemes using the FPGA's CPU or hardware logic.



Results so far, and next steps





Heavy performance dips under sustained access.

Probable bottleneck: A 100 MHz soft-core CPU running an embedded OS is sharing its memory interface with a memory-mapped PCIe IP.

Next steps:
Use dedicated NVMe IP for direct SSD IO.
Use “bare-metal” FPGA configuration.
Develop HDL IP library for common tasks.

Questions? Comments?



FPGA Drive is an adapter that provides NVMe interfaces for FPGA with FMC connectors.



